Cold Electronics Testing

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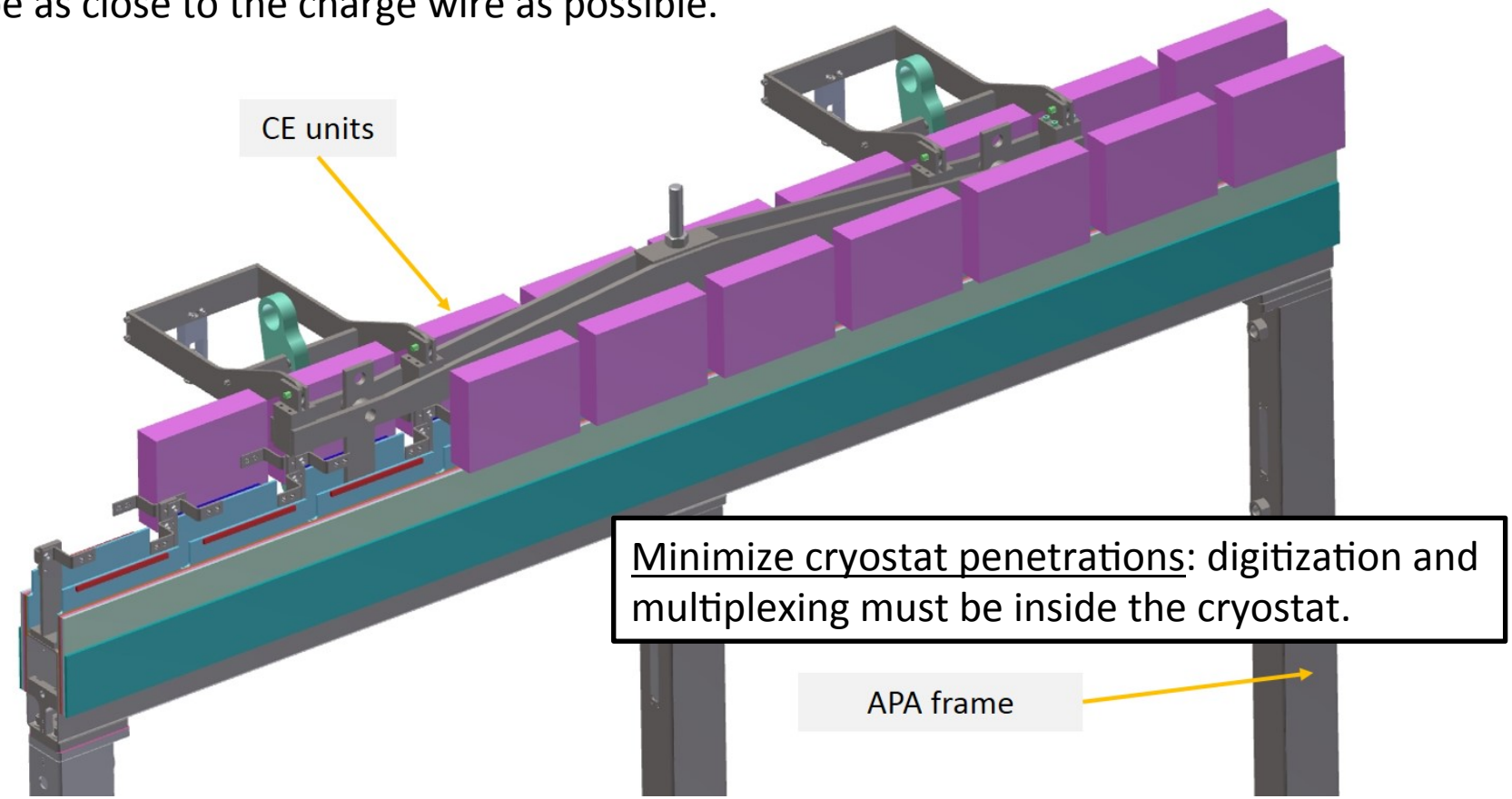
for the CE design and testing team

10/4/16

Why Cold Electronics?

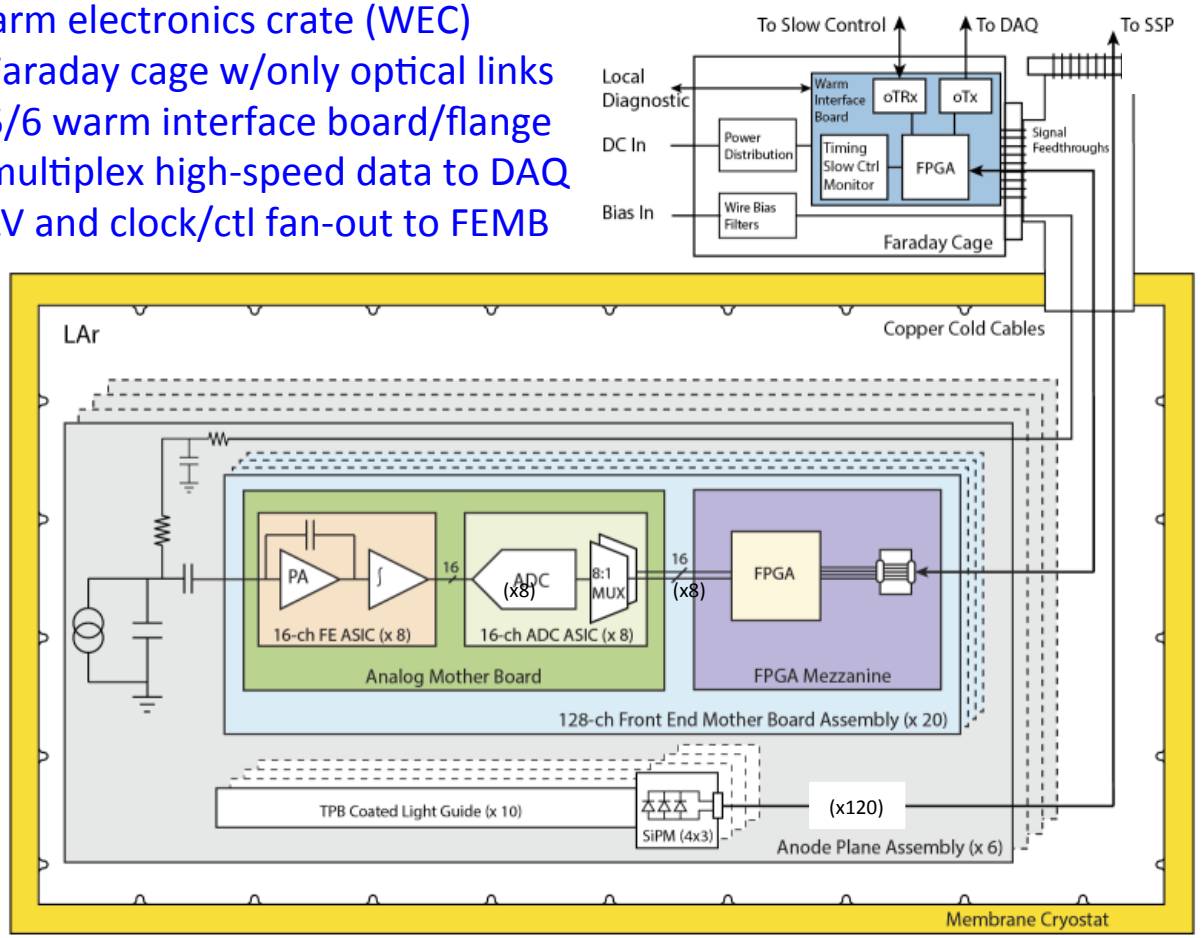
Minimize noise: front end amplification and filtering must be as close to the charge wire as possible.



TPC Cold Electronics

ProtoDUNE shown – SBND has minor differences

Warm electronics crate (WEC)
- Faraday cage w/only optical links
- 5/6 warm interface board/flange
- multiplex high-speed data to DAQ
- LV and clock/ctl fan-out to FEMB



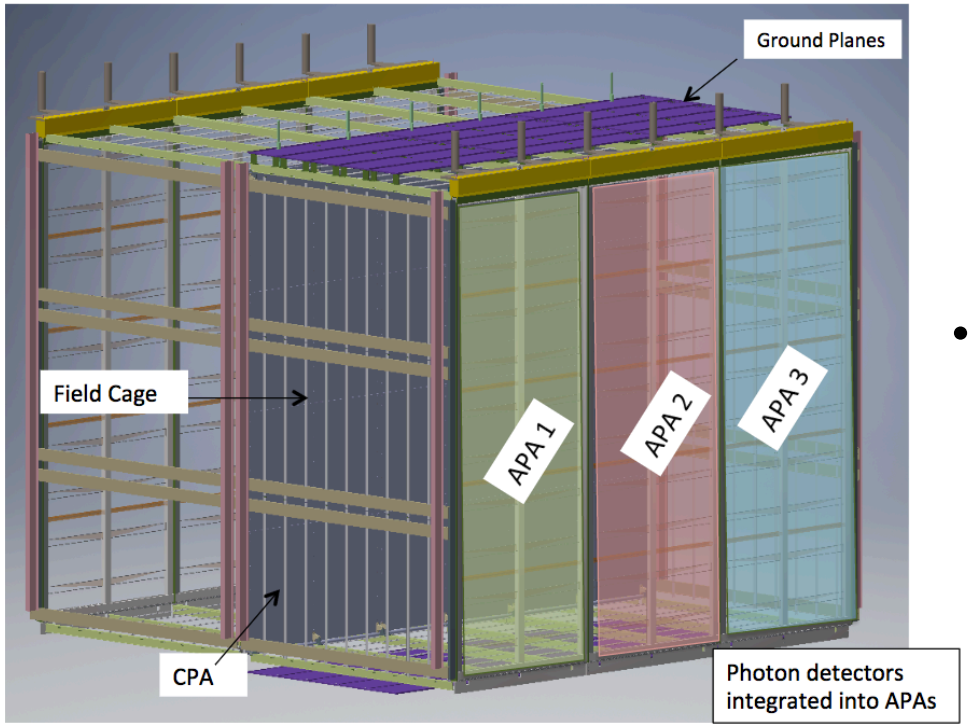
Cryostat feed-through
- 6/4 warm flanges
- 20/24 FEMB/flange

Cold Copper cable
- x120 Samtec 26 AWG
- x88 3M 30 AWG (SBND)

Front-end Mother Board (FEMB) x120 (x88 SBND)
- FE charge amplifier with programmable gain/shaping for each channel
- 12-bit ADC at 2 MS/sec
- 4 x 1.2 Gbps links

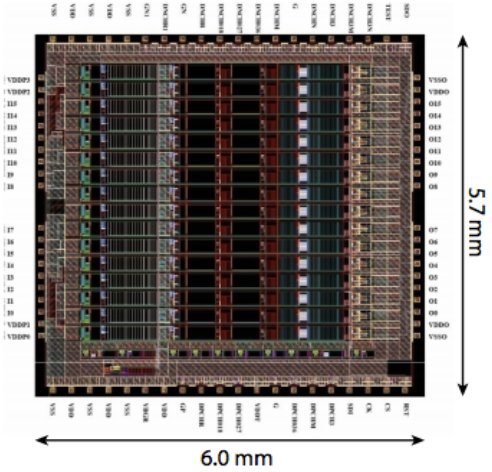
What are all these things?

- Front-end (FE) and ADC ASICs
- FEMBs and cold cable
- Cryostat feed-through and flange
- Warm interface electronics



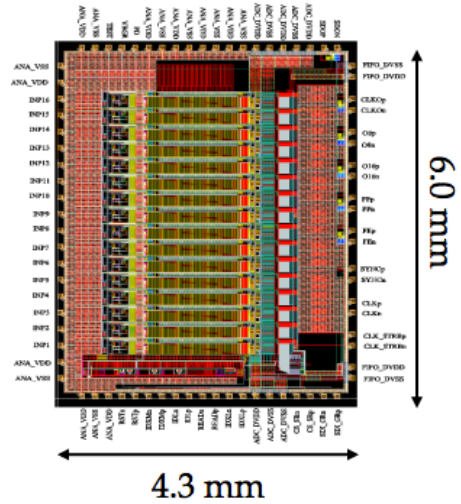
- <u>ProtoDUNE single phase TPC</u>
  - 6 Anode Plane Assemblies (APA) with 2,560 wires each
    - 20 FEMB/APA
    - 2 induction wire planes
    - 1 collection wire plane
  - 7m x 7.2m x 6m
  - 3.6m drift distance with 500V/cm field
- <u>SBND TPC</u>
  - 4 APA joined into 2 units with 5,632 wires each
    - 44 FEMB/joined APA
    - 2 induction wire planes
    - 1 collection wire plane
  - 4m x 5m x 4m
  - 2m drift distance

Cold ASICs



FE

- 16 programmable channels
- Charge amplifier, filter
- Adjustable gain
  - 4.7, 7.8, 14, 25 mV/fC
- Adjustable filter time constant
  - 0.5, 1, 2, 3 µsec peaking time
- Selectable collection/non-collection wire mode
  - 200/900 mV baseline



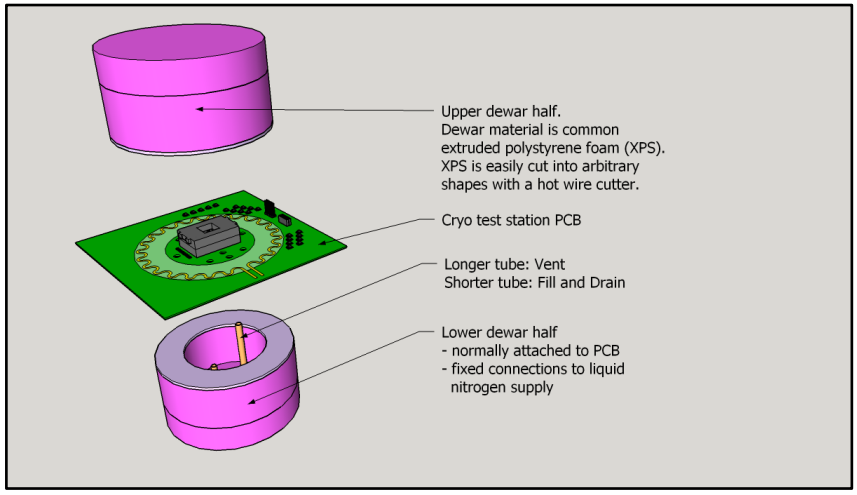
ADC

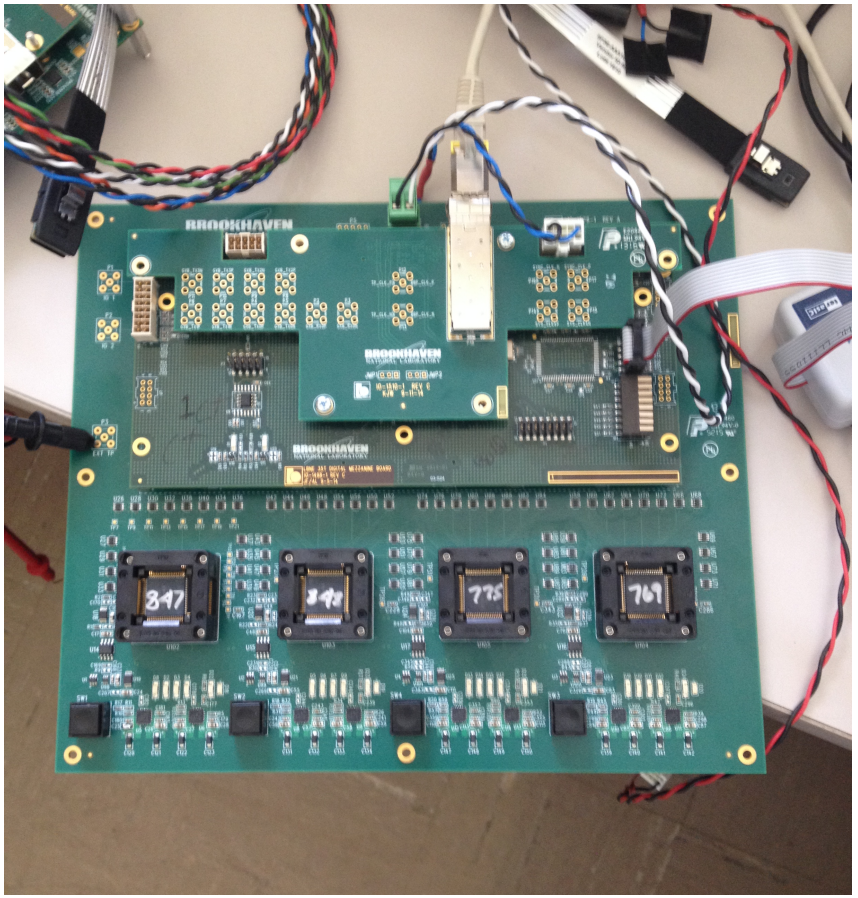
- 16 channels
- 0.2-1.6V input range
- 12-bit ADC sampling at up to 2 MHz
- FIFO 32 samples deep
- multiplexing by 8:1 or 16:1

Requirement: long lifetime (>25 yrs) and very low power consumption in cold.

FE ASIC Testboard

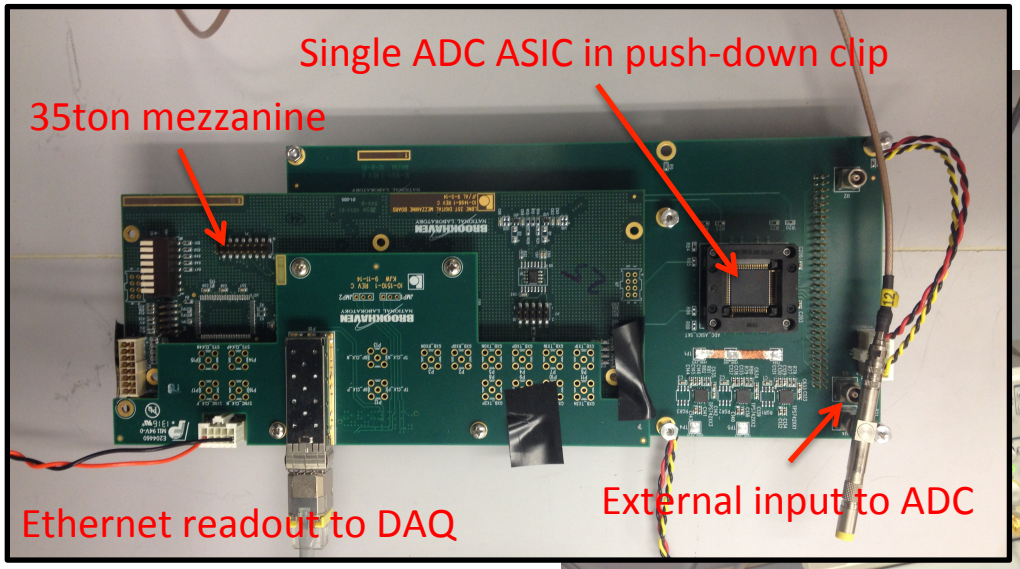
- Prototype FE ASIC test board
  - Controlled by 35ton FPGA mezzanine
  - External DAC
  - 14-bit ADCs
- Read out each FE ASIC on all settings
  - Gain, peaking time, baseline, test capacitor enabled, AC/DC input
  - Also use internal pulser on current P1 version of FE ASICs
- Design for rapid-filling Dewar:

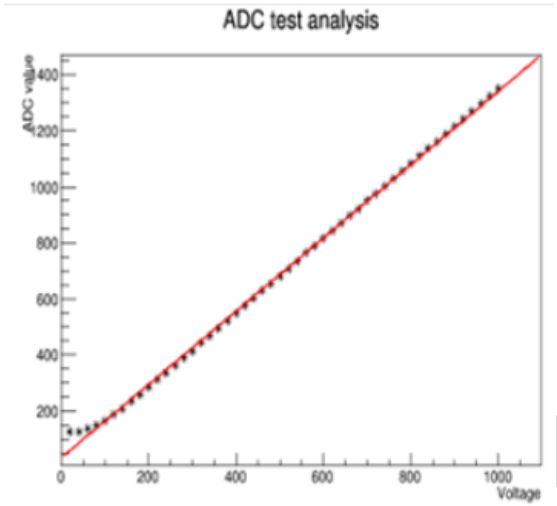


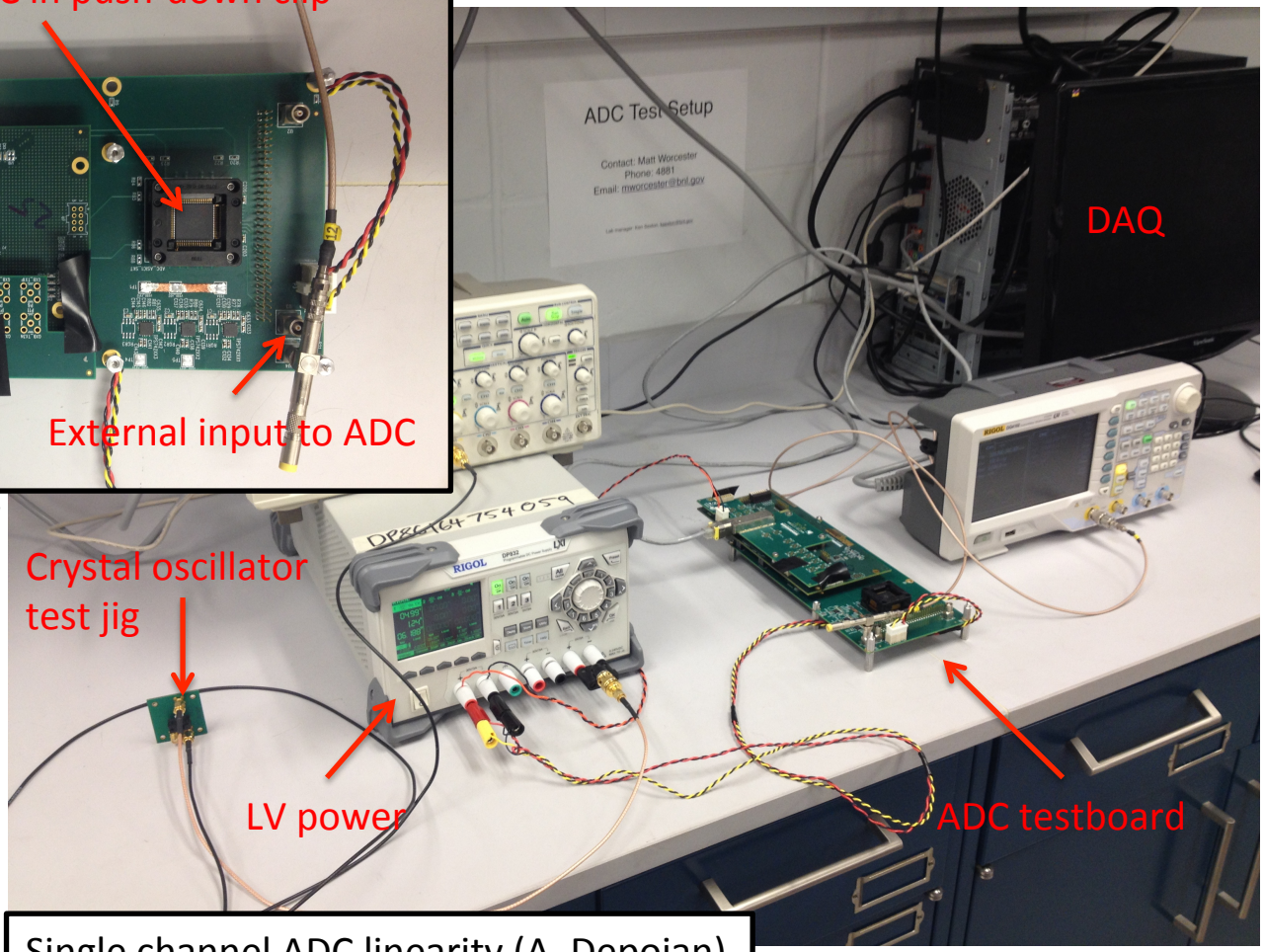


4 FE ASICs in push-down holding clips

ADC ASIC Teststand

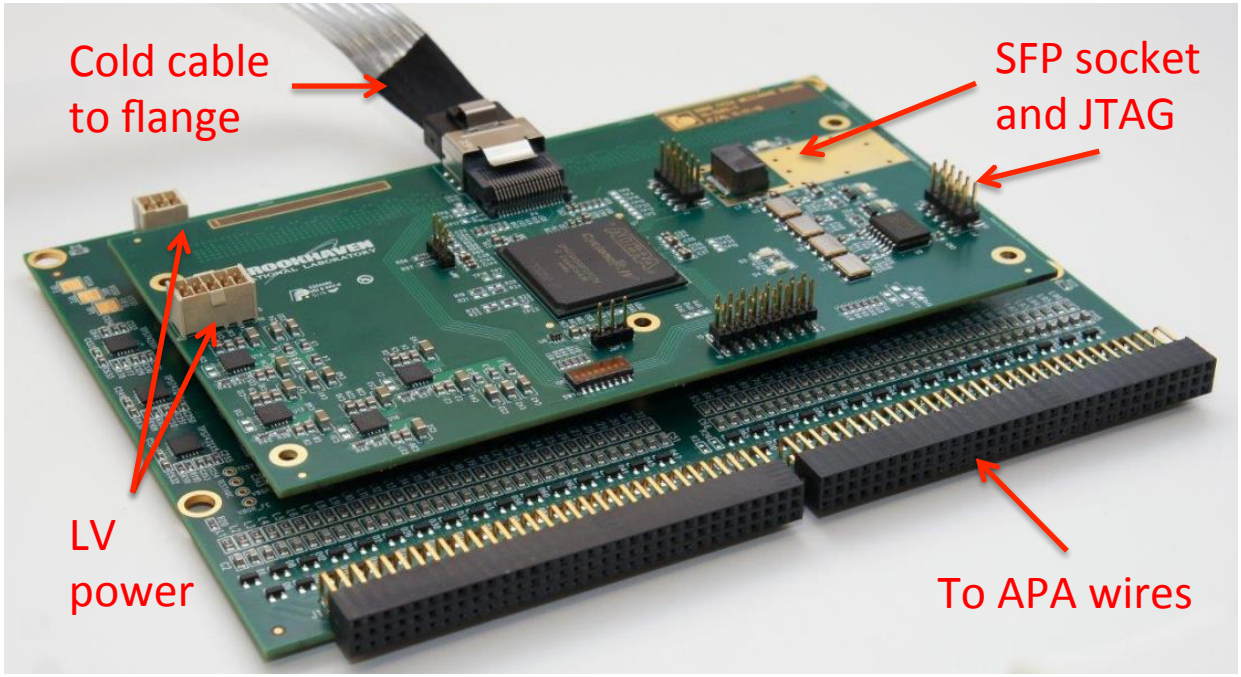


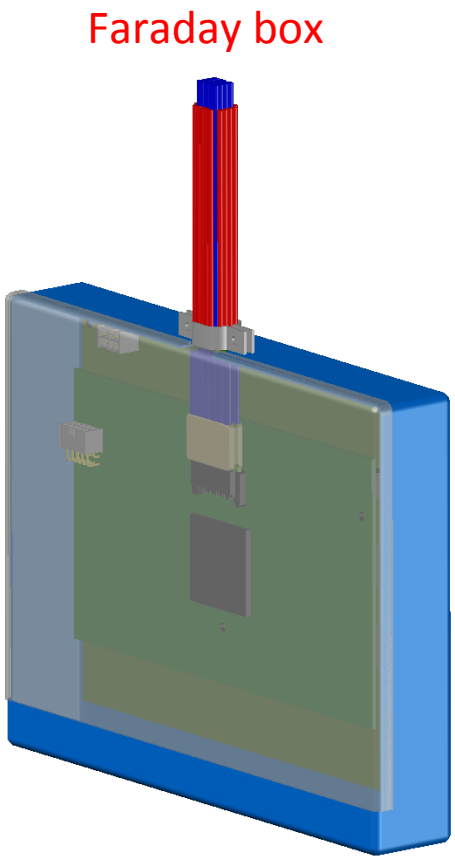




Single channel ADC linearity (A. Depoian)

FEMB

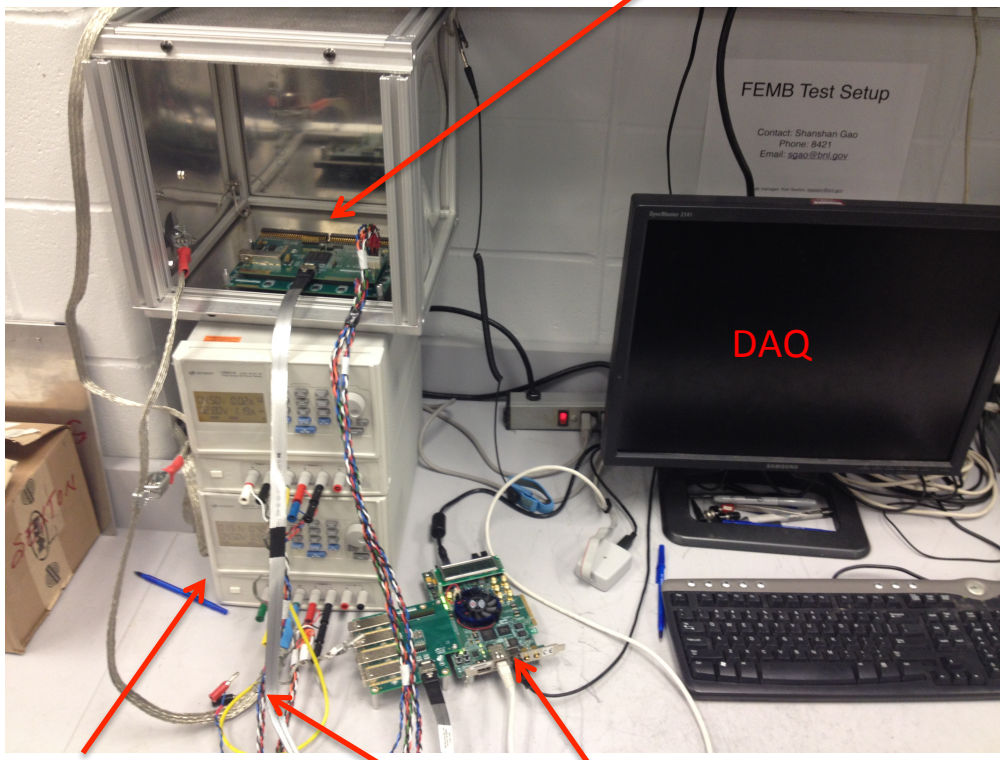




- 128 channels of digitized TPC wire readout
  - 8 FE ASICs/8 ADC ASICs on the analog motherboard
  - Controlled by 2 COLDATA/1 FPGA on the mezzanine
- Mounted in modular Faraday box with built-in cable strain relief

FEMB Teststand

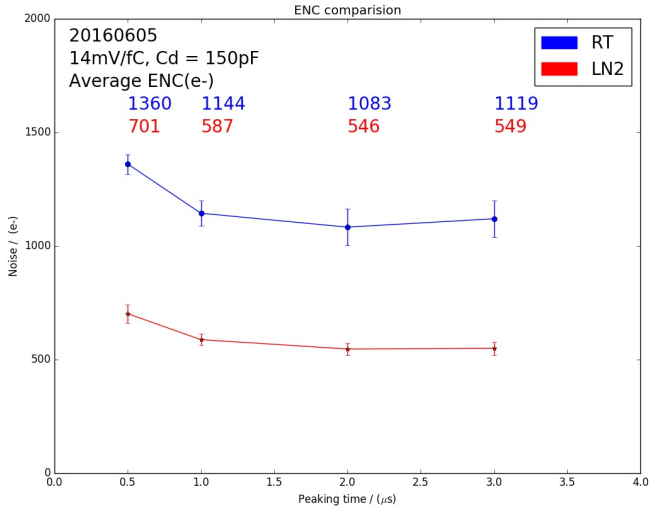
SBND FEMB in Faraday cage

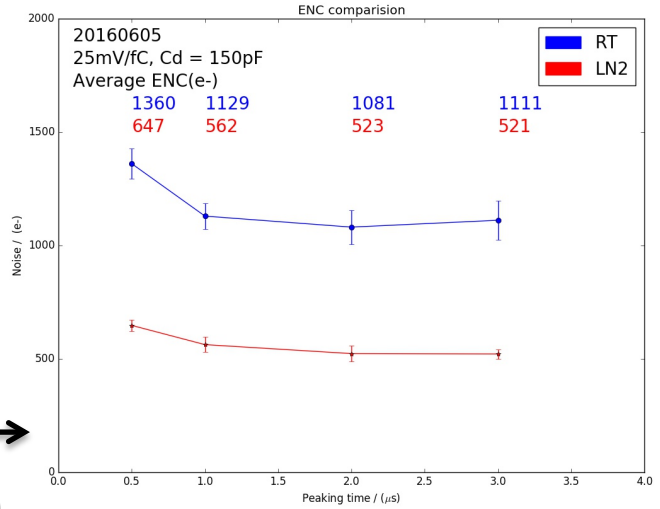


LV power

SBND data cable

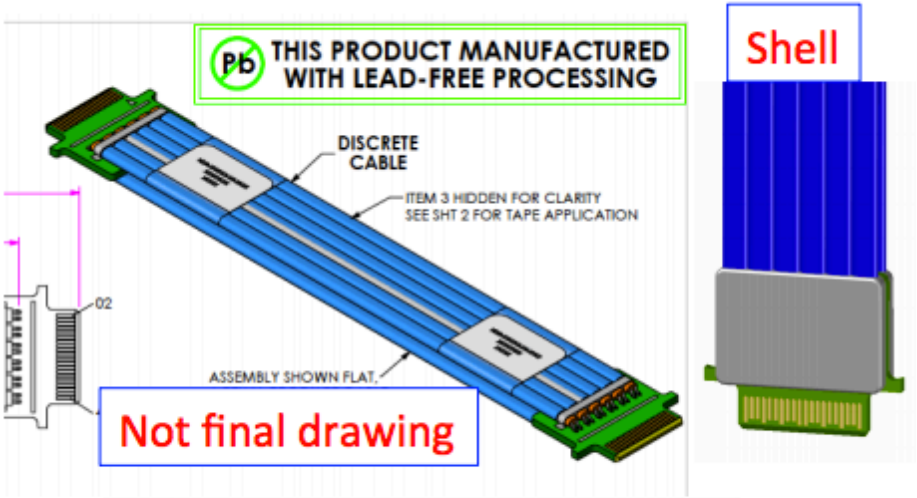
Warm electronics

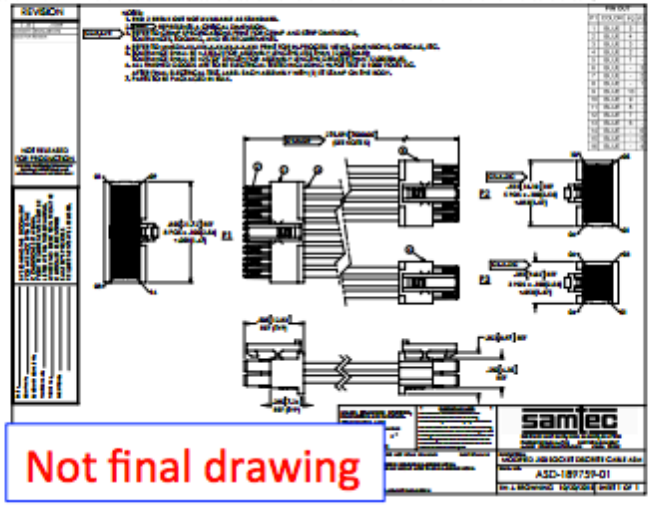




Equivalent Noise Charge (ENC) vs peaking time

Cold Cable Bundles





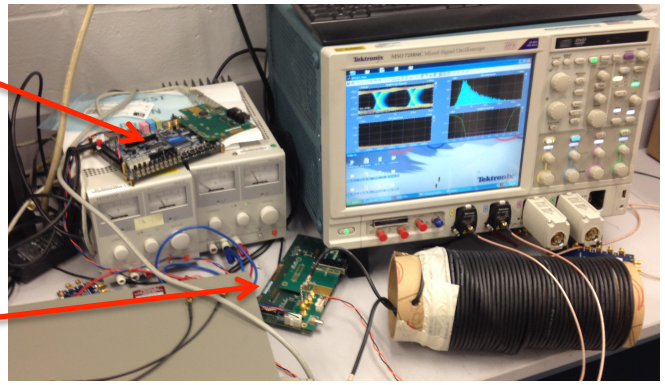
- 4 x 1.2 Gbps high-speed data links from each FEMB to the flange
- Clock, control IO, and FPGA programming links
- 12 pairs of copper twin-axial cable
  - ProtoDUNE: Samtec custom 26 AWG with HSEC08 connectors to both FEMB and flange
  - SBND: 3M mini-SAS with Molex connectors
- LV power: Samtec twisted pair copper wire (16 SBND, 18 ProtoDUNE)

FEMB 7m Cable	Net Name	# of Wires	R_RT [Ω]	R_LAr [Ω]	XSection [mm^2]
Analog Mother Board	FE-ANA-IN	3	0.078	0.025	1.554
	REGR_BIAS	1	0.233	0.074	0.518
FPGA Mezzanine	P1.5V	1	0.233	0.074	0.518
	P2.8V	1	0.233	0.074	0.518
	P3.6V	1	0.233	0.074	0.518
	BIAS	1	0.233	0.074	0.518
Summary		8	0.029	0.009	4.144

Cable Teststand

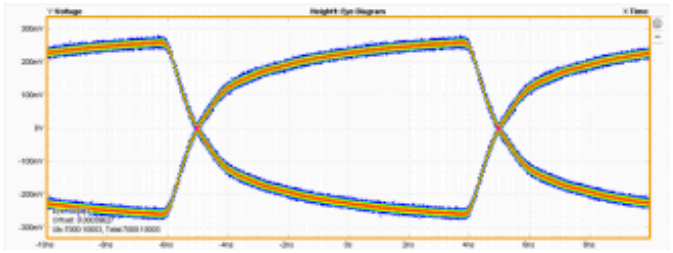
FPGA eval board

35ton FPGA mezzanine

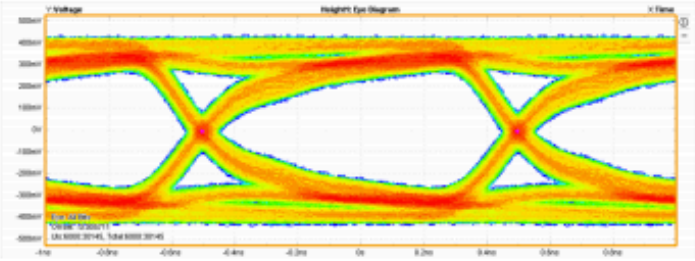


Tektronix oscilloscope

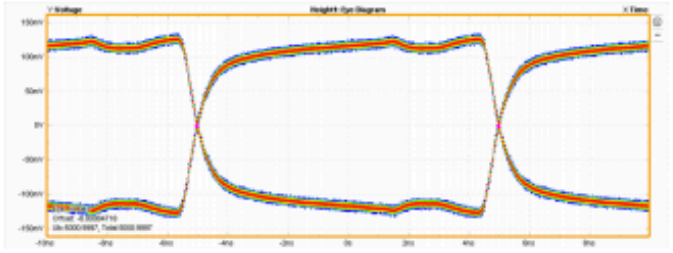
Cable!



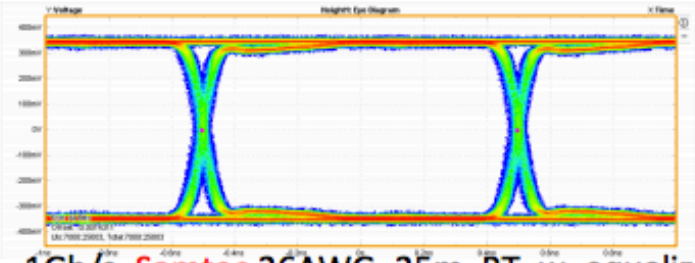
50MHz, Samtec 26AWG, 25m, RT
Height = 415mV, Tj = 180ps



1Gb/s, Samtec 26AWG, 7m, RT, w/o equalizer
Height = 429mV, Tj = 152ps

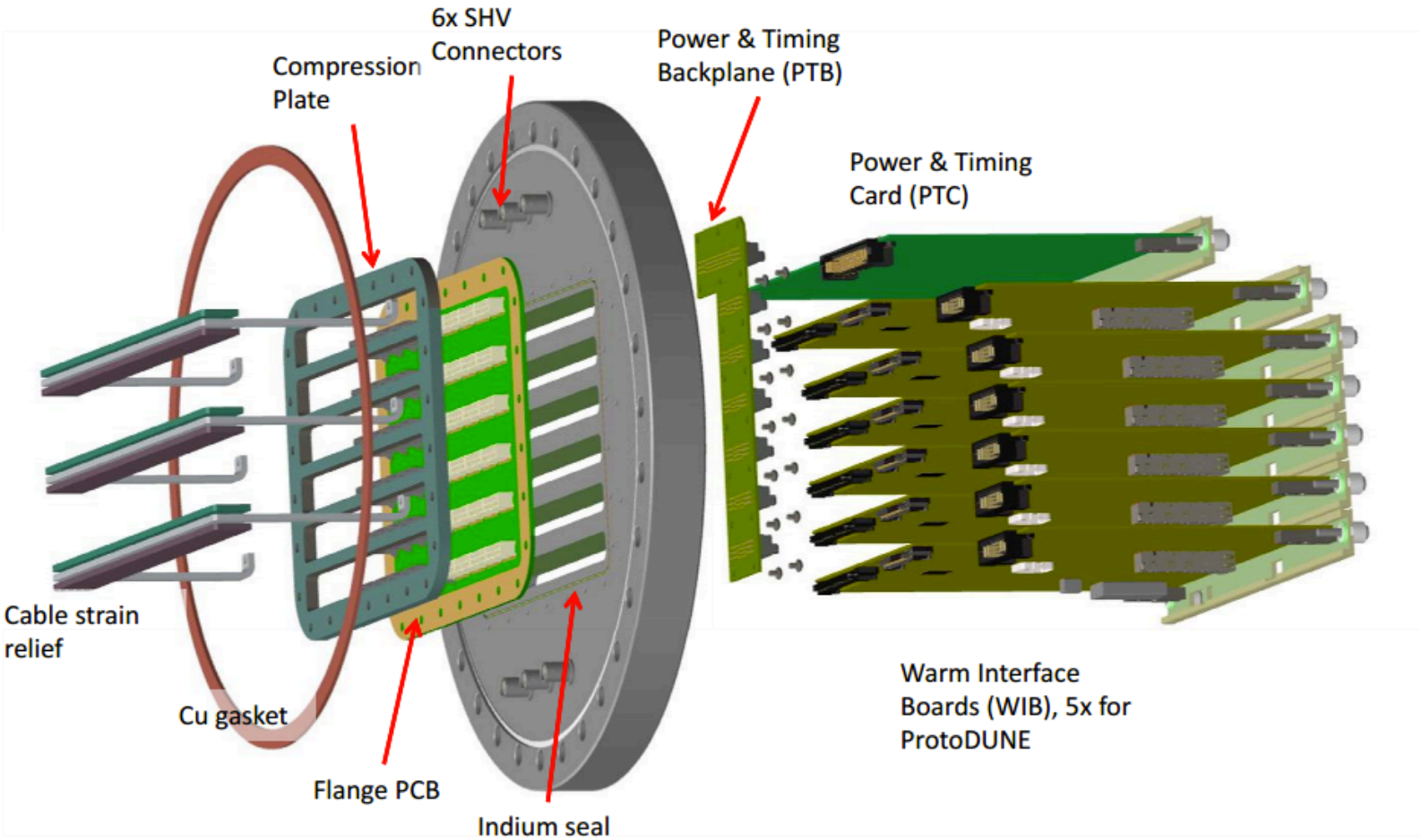


50MHz, Gore 24AWG, 25m, RT
Height = 218mV, Tj = 107ps



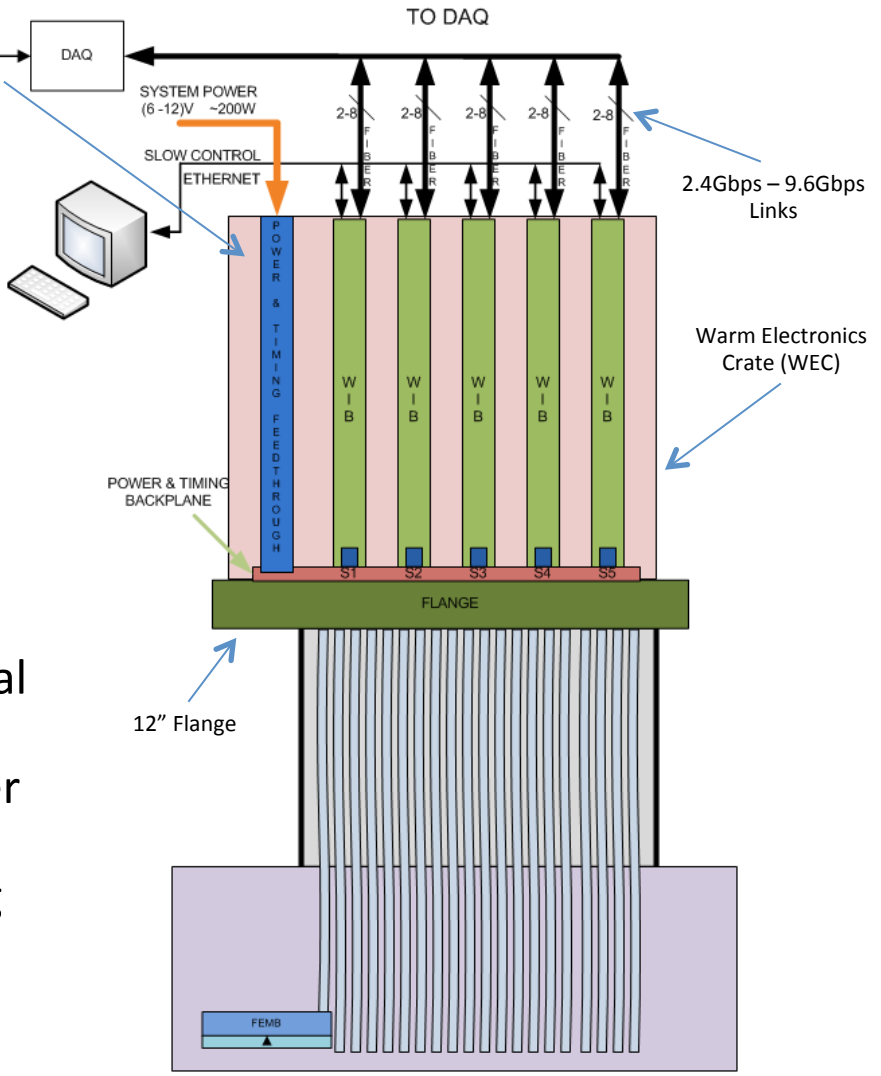
1Gb/s, Samtec 26AWG, 25m, RT, w. equalizer
Height = 628mV, Tj = 113ps

Cold Electronics Flange



Warm Interface Electronics

- One Warm Electronics Crate (WEC) per flange containing:
  - 5/6 Warm Interface Boards (WIB)
    - Each WIB controls up to 4 FEMBs
  - 1 Power and Timing Backplane (PTB)
  - 1 Power and Timing Card (PTC)
- Installed directly onto flange board
  - Receive high-speed data from cold cable
  - Send data to DAQ over 2-8 fiber optical links per WIB
  - Receive 50 clock and sync/control over fiber links to PTC or WIB
  - Interface to slow control system using fiber GIG-E
  - Manage power and control for FEMBs



Integration Teststand

- Full CE readout chain through the warm electronics
  - Use prototype FEMBs
  - Dewar and other cryogenic infrastructure
  - Test warm components
    - Flange
    - Warm interface electronics
    - Cable and connectors
- Goal: full validation of CE through the warm interface
  - Use FELIX PCIe DAQ
  - 10 Gbps Ethernet readout

MicroBooNE prototype integration teststand (Hucheng Chen)

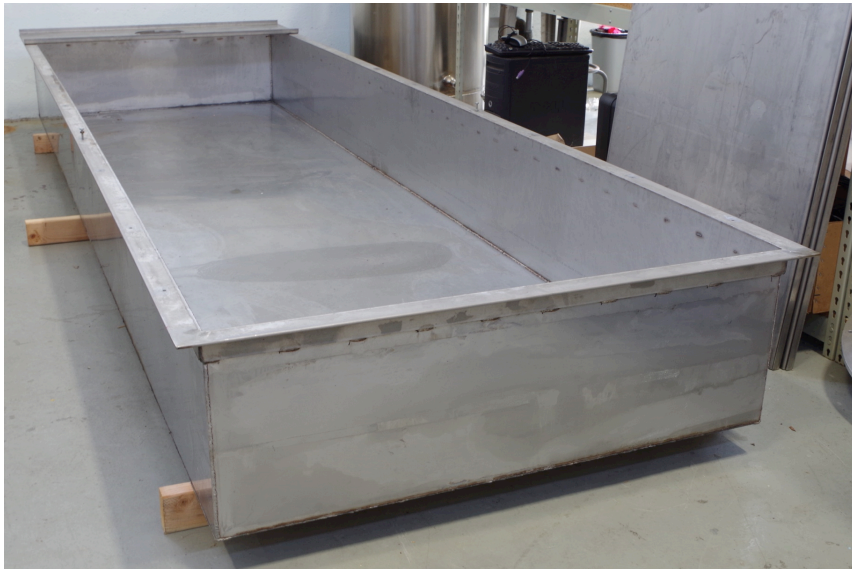
Lab 1-216

- Joint SBND/DUNE testing lab for cold electronics
- Goal: validate all cold electronics for SBND and ProtoDUNE
  - Everything tested here before shipping to CERN or FNAL
- Develop teststands and test procedures for:
  - FE and ADC ASICs
  - Front end motherboards (FEMB)
  - Cryostat feed-through and warm electronics
- Joint effort between BNL and several others: Fermilab, MSU, UTA, Penn

Cold box with 40% APA

Integrated APA+CE+electronics feed-through teststand in the BNL Physics high-bay

- Cold box to submerge FEMB in LN2 (77K)
- Read out via CE flange with WIB/crate
- Bias wires to nominal bias HV



40% prototype APA from PSL with up to 8 FEMB: adapters to CR board with onboard wire bias RC filters already installed